IMAGE REJECT CIRCUIT USING SIGMA-DELTA CONVERSION

ABSTRACT OF THE DISCLOSURE

In a digital IF downconversion circuit, in-phase and quadrature signal components are processed in the form of a single serial digital bit stream through a set of simple logic in combination with a reconstruction filter. A source digital oscillator supplying digital signal mixers employs an oversampled digital word of four bits in length, all of which are binary weighted, to achieve at least sixteen levels of accuracy for a sine wave mixing signal without significant phase or amplitude error. The mixer mixes the digitized serial bit stream according to the clock with output of a four-bit wide table representing the source oscillator and the in-phase and quadrature signals are recombined digitally, followed by binary weighting using weighted resistors coupled into a filter. Thus, image rejection is a digital function which is unaffected by resistor tolerance.

Figure 2

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